Claim Amendments

1-19. (canceled).

20. (original) A comparator comprising;
an input amplifier including:
a first pair of input transistors having a first transistor type, each of the first pair of input transistors being coupled to a corresponding input terminal operable to receive a respective input signal;
a second pair of input transistors having a second transistor type, each of the second pair of input transistors being coupled to a respective one of the corresponding input terminals;
a first current mirror coupled to the first pair of input transistors and operable to sum a first pair of input amplifier output signals and provide at least a portion of a comparator output signal on a comparator output terminal;
a second current mirror coupled to the second pair of input transistors and operable to sum a second pair of input amplifier output signals and provide at least another portion of the comparator output signal on the comparator output terminal;
a first hysteresis transistor including a first hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a first hysteresis current to at least one of the first current mirror and the second current mirror; and
a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a second hysteresis current to at least one of the first current mirror and the second current mirror.

21. (previously presented) The comparator of claim 20, wherein the comparator is integrated within a programmable analog integrated circuit.

22. (previously presented) The programmable analog integrated circuit of claim 21, wherein the integrated circuit comprises:
a plurality of analog circuit blocks;
a plurality of comparators; and
an analog routing pool coupled to the analog circuit blocks and comparators.

23. (currently amended) A comparator comprising;
an input amplifier including:
a first pair of input transistors having a first transistor type, each of the first pair of input transistors being coupled to a corresponding input terminal operable to receive a respective input signal;
a second pair of input transistors having a second transistor type, each of the second pair of input transistors being coupled to a respective one of the corresponding input terminals;
a summing stage coupled to the input amplifier and operable to sum input amplifier output signals and provide a comparator output signal on a comparator output terminal, wherein the summing stage comprises:
a first current mirror coupled to the first pair of input transistors and operable to sum a first pair of input amplifier output signals and provide at least a portion of the comparator output signal on the comparator output terminal; and
a second current mirror coupled to the second pair of input transistors and operable to sum a second pair of input amplifier output signals and provide at least another portion of the comparator output signal on the comparator output terminal; and

a hysteresis feedback stage coupled to the comparator output terminal and operable to supply a hysteresis current to the summing stage.

24. (canceled)

25. (previously presented) The comparator of claim 23, wherein the hysteresis stage comprises:
a first hysteresis transistor including a first hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a first hysteresis current to the summing stage; and
a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a second hysteresis current to the summing stage.

26. (previously presented) The comparator of claim 23, wherein the comparator is integrated within a programmable analog integrated circuit.

27. (previously presented) The programmable analog integrated circuit of claim 26, wherein the integrated circuit comprises:
a plurality of analog circuit blocks;
a plurality of comparators; and
an analog routing pool coupled to the analog circuit blocks and comparators.

28. (previously presented) A comparator comprising;
an input amplifier;
a summing stage including:
a first current mirror coupled to the input amplifier and operable to sum a first pair of input amplifier output signals and provide at least a portion of the comparator output signal on a comparator output terminal; and

a second current mirror coupled to the input amplifier and operable to sum a second pair of input amplifier output signals and provide at least another portion of the comparator output signal on the comparator output terminal; and

a hysteresis feedback stage coupled to the comparator output terminal and operable to supply a hysteresis current to the summing stage.

29. (previously presented) The comparator of claim 28, wherein the hysteresis stage comprises:

a first hysteresis transistor including a first hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a first hysteresis current to at least one of the first current mirror and the second current mirror of the summing stage; and

a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a second hysteresis current to at least one of the first current mirror and the second current mirror of the summing stage.

30. (new) The comparator of claim 28, wherein the comparator is integrated within a programmable analog integrated circuit.

31. (new) The programmable analog integrated circuit of claim 30, wherein the integrated circuit comprises:

a plurality of analog circuit blocks;

a plurality of comparators; and

an analog routing pool coupled to the analog circuit blocks and comparators.